

R16

Code No: 136CH

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, July - 2023

LINEAR AND DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 Hours

Max. Marks: 75

- Note:** i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART-A**(25 Marks)**

- 1.a) Define parameters of Op-Amp.
(i) CMRR (ii) Slew rate (iii) Off-set voltage (iv) Large signal voltage gain. [2]
b) Explain the different methods used to increase the input resistance of an op-amp. [3]
c) What are the characteristics of all pass filter and notch filter? [2]
d) How does PLL work as frequency multiplier? [3]
e) What is the need for A/D and D/A conversion? [2]
f) Find the step size and analog output when input is 1000 and 1111. Assume $V_{ref} = 5V$. [3]
g) Define CMOS Logic levels. [2]
h) Draw the circuit diagram of a half subtractor. [3]
i) Write about Dynamic RAMs and its applications. [2]
j) Discuss how PROM, EPROM and EEPROM technologies differ from each other. [3]

PART-B**(50 Marks)**

- 2.a) Draw the basic block diagram of op-amp and explain the operation of each block.
b) Explain the working of a Schmitt trigger with neat circuit diagram. [5+5]

OR

- 3.a) Explain the working of non-Inverting amplifier and derive the equation of its Gain.
b) Explain the application of three terminal adjustable voltage regulator. [5+5]

- 4.a) Design an active high pass filter with cut-off frequency of 4KHz.
b) How to generate a sawtooth wave form? Explain the working of such a circuit with neat circuit diagram. [5+5]

OR

- 5.a) Explain the operation of Astable multivibrator using 555 timer and also derive the expression for frequency of oscillation.
b) Draw the block diagram of 565 PLL and explain about each block. Make circuit connections to track the input signal and explain its operation. [5+5]

- 6.a) Draw the block diagram of inverted R-2R DAC and explain its operation in detail.
b) With neat schematic, explain the operation of a counter type Analog to Digital converter. [5+5]

OR

- 7.a) Draw the circuit of weighted resistor DAC and derive expression for output analog voltage V_o .
b) Mention ADC characteristics. Calculate the conversion time for a full-scale input in case of a 12-bit counter type ADC driven by 4 MHz clock. [5+5]

- 8.a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.
b) Explain about parity generator and checker. [5+5]

OR

- 9.a) Draw the dynamic electrical behaviour of CMOS inverter and explain.
b) Discuss about 2-input 4-output multiplexer. [5+5]

- 10.a) Draw the circuit of a bidirectional shift register with parallel loading using 2 to 4 line decoder and D-flip-flops.
b) Design an 8×4 diode ROM using 74×138 for the following data starting from the first location. [5+5]

OR

- 11.a) Draw the circuit of MOD 16 Down ripple counter with D-flip-flops and explain its operation.
b) With the help of timing waveforms, explain read and write operations of SRAM. [5+5]

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